REMARKS

In the aforementioned Office Action, claims 1-26 were examined and rejected. In response to the Examiner's remarks regarding claim 1, Applicant is amending claim 1. In view of the foregoing amendment and the following remarks, Applicant hereby respectfully requests reconsideration of the application.

Rejection under 35 U.S.C. § 102

In section 3 of the final Office Action, the Examiner rejected claims 1-11 under 35 U.S.C. § 102(e) as being anticipated by Larson (U.S. Patent No. 6,359,623). Applicant respectfully traverses.

With regard to claim 1, the Examiner stated in section 12, that "Larson's graphics pipeline is a pipeline structure that meets the limitation of 'a pipeline structure' as recited in claim 1." In addition, the Examiner noted that "parallel architecture is not present in the independent claim 1 because the claim limitation only recites a pipeline structure," (section 12). In response, Applicants are amending claim 1 to include in part, "a graphics engine coupled to the memory and comprising a pipeline structure **configured for both sequential and parallel processing** ..."(emphasis added). In support this amendment, the specification states, paragraph 68, lines 1-3, "graphics engine 1006 is a pipeline structure designed to carry out a subdivision process both sequentially and in **parallel**" (emphasis added). Additionally, the specification states, paragraph 72, lines 1-3, "[b]y implementing a pipeline structure ... in which some subdivisions are carried out in parallel, a number of cycles required to determine whether pixels in a tile are inside or outside a primitive is greatly reduced."

Applicant respectfully submits that Larson does not disclose, teach, or suggest a graphics engine including a pipeline structure configured for both sequential and parallel

processing. Specifically, although Larson states, col. 6, lines 19-20, "polygons are being processed through the graphics pipeline," Larson's "graphics pipeline" is not a "pipeline structure configured for both sequential and parallel processing," as claimed in the present invention. As is known in the art, parallel processing typically involves performing a plurality of steps, functions, or processes non-sequentially (i.e., in parallel). An example of a sequential process is a program loop that (under command of a processor) may sequentially compute a specific function for each cell of a plurality of cells, where a cell may be a portion of a display screen, for example. If the plurality of cells is 100, then the processor must perform 100 processing cycles to obtain the specific function for each of the 100 cells. However, if the cells are processed in parallel, either via hardware, software, or a combination, then the processor may compute the 100 functions associated with the 100 cells in one processing cycle.

In contrast, Larson teaches away from a pipeline structure configured for parallel processing. Larson states, col. 10, lines 46-49, "logic can be configured in the hierarchical tiler 57 to implement **nested loops** for the x and y screen space coordinates to group the pixels of the region ..." (emphasis added). Applicant submits that implementation of nested loops is not conducive to parallel processing. Furthermore, Larson discloses, col. 3, lines 17-36, a hierarchical tiler that performs the following steps: (1) subdivides a screen space into a plurality of regions; (2) determines whether each of the regions are entirely inside, entirely outside, or partially inside of a primitive; and (3) converts those regions that are entirely inside the primitive into pixel locations in screen space. The hierarchical tiler then repeats the above steps for each region that is determined to be partially inside the primitive. Larson does not disclose that any of the steps of the hierarchical tiler are performed in parallel. That is, Larson does not disclose a hierarchical tiler that processes information in parallel.

The Examiner stated, section 14, that "the parallel logic circuit is inherently embedded within the hierarchical tiler," since the hierarchical tiler is "configured to update pyramid represented by FIG. 4A-4C," and "process a plurality of pixel locations in screen space." Applicant assumes the Examiner contends that because the hierarchical tiler is configured to perform two separate processes, then the tiler must be implementing some type of parallel logic via an inherently embedded logic circuit. Applicant submits that just because an element (e.g., the tiler) is configured to perform two independent processes, does not imply that the two processes are performed in parallel. In addition, Applicant submits that just because the tiler updates a pyramid and processes a plurality of pixels locations does not imply that the tiler updates the pyramid using parallel processes, or processes the plurality of pixel locations in parallel. In fact, Larsen discloses a hierarchical tiler that processes information only sequentially.

For example, Larson discloses that the hierarchical tiler performs occlusion testing on polygons using z values stored in a pyramid data structure, and that a coverage mask associated with a level of the pyramid may need to be updated. However, Larson does not disclose that any of the occlusion testing or coverage mask updating processes are parallel processed. For example, Larson discloses, col. 9, lines 35-44, "when the bits for all of the subregions associated with a region have been set in a coverage mask, the coverage mask associated with the next level up in the pyramid will need to be set. The process then proceeds to the next level up in the pyramid and a determination is then made as to whether the coverage mask associated with that level up in the pyramid needs to be set. This process continues until either the top level of the pyramid is reached or a determination is made that the corresponding bits in the coverage mask do not need to be set." It is obvious that Larson discloses sequential processes (i.e., setting bits of a

coverage mask one level at a time) for updating coverage masks associated with the pyramid.

Larson discloses that the hierarchical tiler may perform a scan conversion process in conjunction with occlusion testing (col. 5, lines 13-19). For example, Larson discloses, col. 11, line 17 – col. 12, line 3, the following **sequential** steps: (1) determine if all the corners of a (N x N) region are outside of a primitive; (2) if all the corners of the region are not outside of the primitive, determine if all the corners of the region are inside the primitive; (3) if all the corners are inside the primitive, then determine if the primitive is occluded; (4) if all the corners are not inside the primitive, determine if the region is at least partially covered by the primitive; (5) if the region is at least partially covered by the primitive, then determine if the primitive is occluded; and (6), if the primitive is not occluded, then subdivide the region into a plurality of regions. The process then repeats at step (1) for each of a plurality of regions. Applicant submits that it is clear that Larson discloses a hierarchical tiler that **sequentially** performs scan conversion in conjunction with occlusion testing, as is evident in the disclosed **sequential** steps in which the results of one step must be obtained before the next step is initiated. If the Examiner believes that Larson discloses a hierarchical tiler that either comprises parallel logic or processes steps in parallel, then the Applicant respectfully requests that the Examiner point out specific passages in Larson that support such a belief.

Therefore, based at least upon the above remarks, Applicant submits that amended claim 1 is not anticipated by Larson, and respectfully requests that claim 1 be allowed. Furthermore, since claims 2-11 depend directly or indirectly from claim 1, Applicant submits that claims 2-11 are allowable for at least the same reasons as claim 1. In addition, claim 4 is allowable because Larson does not disclose a pipeline structure that determines "whether the polygonal portion of the raster image is at least **partly inside** the

graphics primitive by evaluation of **edge functions of the graphic primitive,**" as claimed (emphasis added). In contrast, Larson discloses a method that determines whether a region is partially covered by a graphics primitive (i.e., whether the region is partially inside the graphics primitive) by calculating plane equations for each edge of a bounding box that encloses the primitive (col. 13, lines 5-51; FIG. 11). That is, Larson evaluates **edge functions of the bounding box**, but does **not** disclose using **edge functions of the enclosed primitive** to determine if the region is partially covered by the graphics primitive.

Rejection under 35 U.S.C. § 103

In section 6 of the final Office Action, the Examiner rejected claims 12-26 under 35 U.S.C. § 103(a) as being unpatentable over Larson in view of Greene et al. (U.S. Patent No. 6,480,205). Applicant respectfully traverses.

With regard to claim 12, the Examiner asserts in section 7, subsections 2-3, that it is not clear whether Larson teaches using a coordinate reference frame located at the geometric center of a region or an area corresponding to the portion of the claimed invention, but Greene et al. teaches implicitly a reference frame located at a geometric center of the tile, (see Greene et al., FIG. 2).

Greene et al.'s FIG. 2 illustrates a three level z-pyramid comprising a z-buffer for each level. The finest level 212 of the z-pyramid contains depths of the nearest primitive encountered so far at each image point, and each higher level (i.e., coarser level) contains the largest depths within corresponding square regions of a lower finer level (col. 8, lines 24-67). However, contrary to the Examiner's assertion that a reference frame is located at the center of the tile, Greene et al. explicitly discloses that the reference frames are located at the lower left corner of the tiles. For example, reference frame 222 (FIG. 2)

and reference frame 224 (FIG. 2) are located at the lower left corner of tiles 210 (FIG. 2) and 220 (FIG. 2), respectively. In addition, Greene et al. states, col. 14, lines 40-41, "FIG. 2 shows the coordinate frames (e.g., 222, 224) of the eight 4 x 4 tiles." Furthermore, with regard to FIG. 10, Greene et al. states, col. 14, lines 26-27, "[t]he origin of the coordinate frame is located at the tile's lower-left corner 1002." Applicants submit that it is clear that Greene et al.'s coordinate reference frames are **not** located at the geometric center of the corresponding tiles, and thus Greene et al. does not disclose "using a coordinate reference frame located at a geometric center of the polygonal portion," as claimed.

In addition, the Examiner stated, section 7, subsection 4, that "Larsen suggests selecting a reference frame (figure 11) with a reference point that may be the geometric center of the regions (Larson column 11, lines 1-15)." However, upon inspection of the above-referenced passage of Larsen, Applicant fails to see any evidence that Larson suggests selecting a reference frame with a reference point that may be the geometric center of a region. In fact, in the passage cited above, Larson does not discuss reference frames or geometric centers of regions. Applicant respectfully requests that the Examiner either withdraw the statement, or clearly explain which portion of Larson's text suggests selecting a reference frame with a reference point that may be the geometric center of a region.

Based at least upon the above remarks, Applicant submits that claim 12 is not obvious over Larson in view of Greene et al., and respectfully requests that claim 12 be allowed. Furthermore, since claims 13-19 depend directly or indirectly from claim 12, Applicant submits that claims 13-19 are allowable for at least the same reasons as claim 12, and requests that claims 13-19 be allowed.

Claims 20, 22, and 26 recite a limitation similar to claim 12, as discussed above. Therefore, based at least on the above reasons given in conjunction with claim 12, Applicant submits that claims 20, 22, and 26 are allowable, and requests that claims 20, 22, and 26 be allowed. Furthermore, since claim 21 depends from claim 20, and claims 23-25 depend from claim 22, Applicant submits that claim 21 and claims 23-25 are allowable for at least the same reasons that claims 20 and 22 are allowable, respectively. Therefore, Applicant requests that claims 21 and 23-25 be allowed.

Based on the foregoing remarks, Applicant believes that the rejections in the Office Action of August 28, 2003 are fully overcome, and that the Application is in condition for allowance. If the Examiner has questions regarding the case, he is invited to contact Applicant's undersigned representative at the number given below.

Respectfully submitted,

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